CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A delay circuit, comprising:

a first circuit including:

a circuit input to receive a reference signal;

a circuit output to output a delayed signal being a delayed response to the reference signal;

a logic circuit including a logic input and a logic output, the logic input coupled to the circuit input to generate an inversion of the reference signal at the logic output;

a pull up path coupled to the logic output; and

a pull down path coupled to the logic output;

a falling edge delay circuit coupled to the pull up path to control delay of a falling edge of the reference signal, wherein the pull up path includes a first transistor to selectively couple the logic output to the falling edge delay circuit; and

a rising edge delay circuit coupled to the pull down path to control delay of a rising edge of the reference signal, wherein the pull down path includes second and third transistors coupled in series to selectively couple the logic output to the rising edge delay circuit.

2. (Previously Presented) The delay circuit of claim 1, wherein the first circuit comprises an enable circuit and wherein the logic circuit further includes an enable input to receive an enable signal for enabling the delay circuit.

3. (Original) The delay circuit of claim 2, wherein the circuit input comprises a clock input to receive a reference clock signal and the reference signal comprises the reference clock signal.

4. (Previously Presented) The delay circuit of claim 2, wherein the falling edge delay circuit and the rising edge delay circuit are coupled to delay the falling edge and the rising edge independently of each other.

5. (Previously Presented) The delay circuit of claim 4, wherein the falling edge delay circuit is further coupled to selectively delay the falling edge of the reference signal by variable falling delays and wherein the rising edge delay circuit is further coupled to selectively delay the rising edge of the reference signal by variable rising delays.

6. (Original) The delay circuit of claim 5, wherein the falling edge delay circuit further comprises falling delay inputs to receive falling delay signals, the falling edge delay circuit to select one of the variable falling delays based on the falling delay signals and wherein the rising edge delay circuit further comprises rising delay inputs to receive rising delay signals, the rising edge delay circuit to select one of the variable rising delays based on the rising delay signals.

7. (Previously Presented) The delay circuit of claim 5, wherein the falling edge delay circuit is further coupled to selectively delay the falling edge of the reference signal by one of four falling delays in linear increments, and wherein the rising edge delay circuit is further coupled to selectively delay the rising edge of the reference signal by one of four rising delays in linear increments.

8. (Previously Presented) The delay circuit of claim 2, wherein the enable circuit further includes an inverter coupling the logic output to the circuit output and wherein, the logic circuit comprises a NAND logic gate including first and second NAND inputs and a NAND output, the first NAND input corresponding to the logic input, the second NAND input corresponding to the enable input, and the NAND output corresponding to the logic output.

9. (Previously Presented) The delay circuit of claim 8, wherein the falling edge delay circuit comprises three parallel pull up paths each including at least one transistor to be coupled between a supply voltage and the pull up path of the enable circuit, each one of the three parallel pull up paths responsive to the falling delay signals to select one of the variable falling delays.

10. (Previously Presented) The delay circuit of claim 8, wherein the rising edge delay circuit comprises three parallel pull down paths each including at least one transistor to be coupled between a ground voltage and the pull down path of the enable circuit, each one of the three parallel pull down paths responsive to the rising delay signals to select one of the variable rising delays.

11. (Previously Presented) A delay circuit, comprising:

an inverting enable circuit including:

a circuit input to receive a reference signal;

a circuit output to output a delayed signal being a delayed inversion of the reference signal;

a logic circuit including a logic input and a logic output;

a first inverter coupling the circuit input to the logic input;

a pull up path coupled to the logic output;

a pull down path coupled to the logic output; and

an second inverter coupling the logic output to the circuit output; and

a falling edge delay circuit coupled to the pull down path to control delay of a falling edge of the reference signal; and

a rising edge delay circuit coupled to the pull up path to control delay of a rising edge of the reference signal.

12. (Previously Presented) The delay circuit of claim 11, wherein the logic circuit comprises a NAND logic gate including first and second NAND inputs and a NAND output, the first NAND input corresponding to the logic input, the second NAND

input coupled to an enable input, and the NAND output corresponding to the logic output.

13. (Previously Presented) The delay circuit of claim 12, wherein:

the rising edge delay circuit comprises three parallel pull up paths each including at least one transistor to be coupled between a supply voltage and the pull up path of the inverting enable circuit, each one of the three parallel pull up paths responsive to rising delay inputs of the rising edge delay circuit to select one of variable falling delays of the output delayed signal; and

the falling edge delay circuit comprises three parallel pull down paths each including at least one transistor to be coupled between a ground voltage and the pull down path of the inverting enable circuit, each one of the three parallel pull down paths responsive to falling delay inputs of the falling edge delay circuit to select one of variable rising delays of the output delayed signal.

14. (Previously Presented) A machine-accessible medium having contained thereon a description of an integrated circuit, the integrated circuit comprising:

a clock enable circuit including:

a clock input to receive a reference clock signal;

an enable input;

a circuit output to output a delayed clock signal being a delayed response to the reference clock signal;

a NAND logic circuit having a first NAND input coupled to receive the reference clock signal, a second NAND input coupled to the enable input, and a NAND output; and

an inverter circuit coupling the NAND output to the circuit output;

a falling edge delay circuit coupled to the enable circuit to control delay of a falling edge of the reference clock signal; and

a rising edge delay circuit coupled to the enable circuit to control delay of a rising edge of the reference clock signal.

15. (Original) The machine-accessible medium of claim 14, wherein the falling edge delay circuit and the rising edge delay circuit are coupled to delay the falling edge and the rising edge independently of each other.

16. (Original) The machine-accessible medium of claim 15, wherein the falling edge delay circuit is further coupled to selectively delay the falling edge of the reference clock signal by variable falling delays and wherein the rising edge delay circuit is further coupled to selectively delay the rising edge of the reference clock signal by variable rising delays.

17. (Original) The machine-accessible medium of claim 16, wherein the falling edge delay circuit further comprises falling delay inputs to receive falling delay signals, the falling edge delay circuit to select one of the variable falling delays based on the falling delay signals and wherein the rising edge delay circuit further comprises rising delay inputs to receive rising delay signals, the rising edge delay circuit to select one of the variable rising delays based on the rising delay signals.

18. (Original) The machine-accessible medium of claim 16, wherein the falling edge delay circuit is further coupled to selectively delay the falling edge of the reference clock signal by one of four falling delays in linear increments, and wherein the rising edge delay circuit is further coupled to selectively delay the rising edge of the reference clock signal by one of four rising delays in linear increments.

19. (Previously Presented) The machine-accessible medium of claim 17, wherein the clock enable circuit further comprises:

a first pull up path including a first transistor to selectively couple the NAND output to the falling edge delay circuit; and

a pull down path including second and third transistors coupled in series to selectively couple the NAND output to the rising edge delay circuit.

20. (Original) The machine-accessible medium of claim 19, wherein the falling edge delay circuit comprises three parallel pull up paths each responsive to the falling delay signals to select one of the variable falling delays, and wherein the rising edge delay circuit comprises three parallel pull down paths each responsive to the rising delay signals to select one of the variable rising delays.

21. (Original) The machine-accessible medium of claim 14, wherein the description comprises one of hardware behavioral code, register transfer level code, a netlist, and a circuit layout.

22. (Previously Presented) An integrated circuit, comprising:

a clock distribution network to distribute a reference clock signal throughout the integrated circuit;

clock delay circuits each comprising:

a clock enable circuit including:

a clock input to receive the reference clock signal;

an enable input;

a circuit output to output a delayed clock signal being a delayed response to the reference clock signal;

a NAND logic circuit having a first NAND input coupled to receive the reference clock signal, a second NAND input coupled to the enable input, and a NAND output; and

an inverter circuit coupling the NAND output to the circuit output;

a falling edge delay circuit coupled to the enable circuit to control delay of a falling edge of the reference clock signal; and

a rising edge delay circuit coupled to the enable circuit to control delay of a rising edge of the reference clock signal;

latches each clocked according to the delayed clock signal output from each of the clock delay circuits; and

logic clusters to compute logic values, the latches coupled to buffer the logic values between clock edges of the delayed clock signals.

23. (Original) The integrated circuit of claim 22, wherein the falling edge delay circuit and the rising edge delay circuit are coupled to delay the falling edge and the rising edge independently of each other.

24. (Original) The integrated circuit of claim 22, wherein the falling edge delay circuit further comprises falling delay inputs to receive falling delay signals, the falling edge delay circuit to selectively delay the falling edge of the reference clock signal by one of variable falling delays based on the falling delay signals, and wherein the rising edge delay circuit further comprises rising delay inputs to receive rising delay signals, the rising edge delay circuit to selectively delay the rising edge of the reference clock signal by one of the variable rising delays based on the rising delay signals.

25. (Original) The integrated circuit of claim 24, wherein the clock delay circuits are grouped into domains of the integrated circuit, the falling delay inputs and the rising delay inputs of the clock delay circuits coupled to receive the same falling delay signals and the same rising delay signals within each of the domains.

26. (Original) The integrated circuit of claim 24, wherein the falling edge delay circuit is further coupled to selectively delay the falling edge of the reference clock signal by one of four falling delays in first increments, and wherein the rising edge delay circuit is further coupled to selectively delay the rising edge of the reference clock signal by one of four rising delays in second increments.

27. (Original) The integrated circuit of claim 26, wherein the first and second increments comprise substantially linear increments.

28. (Original) The integrated circuit of claim 22, wherein the integrated circuit comprises a microprocessor.

29. (Original) The integrated circuit of claim 22, wherein the logic clusters comprise at least one of combinational logic and sequential logic.

30. (Previously Presented) The integrated circuit of claim 23, wherein the clock enable circuit comprises:

a first pull up path including a first transistor to selectively couple the NAND output to the falling edge delay circuit; and

a pull down path including second and third transistors coupled in series to selectively couple the NAND output to the rising edge delay circuit.

31. (Original) The integrated circuit of claim 30, wherein the falling edge delay circuit comprises three parallel pull up paths each responsive to the falling delay signals to select one of the variable falling delays, and wherein the rising edge delay circuit comprises three parallel pull down paths each responsive to the rising delay signals to select one of the variable rising delays.

32. (Original) The integrated circuit of claim 22, wherein the latches comprise flip-flops.

33. (Previously Presented) The machine-accessible medium of claim 14, wherein the clock enable circuit comprises an inverting clock enable circuit and wherein the inverting clock enable circuit further includes an inverter coupled between the clock input and the first NAND input.

34. (Previously Presented) The delay circuit of claim 1, wherein gates of the first and third transistors are coupled to the logic input of the logic circuit.

35. (Previously Presented) The delay circuit of claim 2, wherein a gate of the second transistor is coupled to the enable input.

36. (Previously Presented) The delay circuit of claim 11, wherein the pull up path includes a first transistor to selectively coupled the logic output to the rising edge delay circuit and wherein the pull down path includes second and third transistors coupled in series to selectively coupled the falling edge delay circuit to the logic output.

37. (Previously Presented) The delay circuit of claim 36, wherein the gates of the first and third transistors are coupled to the logic input of the logic circuit and wherein a gate of the second transistor is coupled to an enable input.